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Abstract

By selecting a high quality GaAs epitaxial wafer and reducing parasitics, packaged FETs with NF_{min} of 2.4 dB and G_a of 7.5 dB at 18 GHz were produced. Using these FETs, a single stage amplifier with NF of 2.7 dB and G of 6.4 dB at 18 GHz was constructed.

Introduction

Facing the age of SHF TV broadcasting and satellite telecommunication, super low noise GaAs FETs operating at above X band frequencies are strongly required. In this frequency region, however, high performance has been so far obtained only by a chip device⁽¹⁾. When reliability and handling feasibility are considered, packaged devices are preferred.

Authors developed high performance packaged GaAs FETs for Ku band operation. In the process, attention was especially paid for selection of a high quality GaAs epitaxial wafer and reduction of undesirable parasitics of the devices.

Developed devices showed the minimum noise figure (NF_{min}) of 1.3 dB and the associated gain (G_a) of 11 dB at 12 GHz, and NF_{min} of 2.4 dB and G_a of 7.5 dB at 18 GHz. Using these devices, a single stage amplifier with NF of 2.7 dB and G of 6.4 dB at 18 GHz were constructed.

GaAs Epitaxial Wafer

A large mutual conductance around pinch off current and the least leakage current at the pinch off are important. As these are sensitive factors of the crystal quality and electrical characteristics of the semiinsulating buffer layer and the active layer at the buffer layer-active layer interface,

- (1) abruptness of the carrier profile at the interface was controlled and the density and the gradient of the carrier profile in the active layer were optimized⁽²⁾, and
- (2) method to select an epitaxial wafer having a small density of deep level impurity was developed.

FETs were fabricated using GaAs epitaxial wafers with different light sensitivity of the buffer layer. NF_{min} and the linear power gain (G_L) of FETs were evaluated as a function of the light sensitivity ratio (R_D / R_B), where R_B is the resistance under 100 Lux light illumination and R_D , under dark condition.

From Fig. 1, it is found that NF_{min} rapidly increases and G_L slightly decreases with increases of $\log(R_D / R_B)$.

This light sensitivity is attributed to the deep level impurities, a high quality GaAs epitaxial wafer with the least

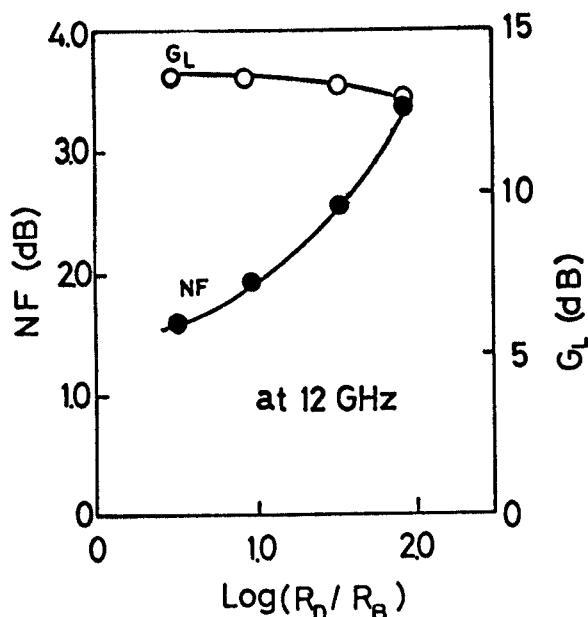


Fig. 1 NF_{min} and G_L depending on a function of the light sensitivity ratio, R_D / R_B .

sensitivity is absolutely necessary for super low noise GaAs FETs.

FET Design and Fabrication

Loss of RF signal in gate electrode rapidly increases at higher frequencies. As this resistance is mainly determined by the gate resistance (R_g), the gate length (L_g) and the gate to source capacitance (C_{gs}), followings were especially considered in designing devices.

- (1) Shortening of the unit gate width (W_{gu}) to reduce C_{gs} and decrease R_g .
- (2) Optimizing of the carrier density correlating to C_{gs} .

From the investigation using FETs with different W_{gu} , W_{gu} was optimized to be 75 μm as shown in Fig. 2. The total gate width was determined to be 300 μm (75 $\mu m \times 4$) not to introduce degradation of FETs performance by phase delay depending on lateral spreading.

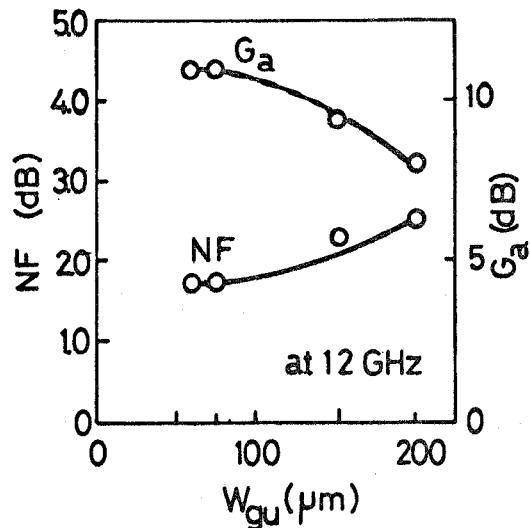


Fig. 2 NF_{min} and G_a against the unit gate width, W_{gu} .

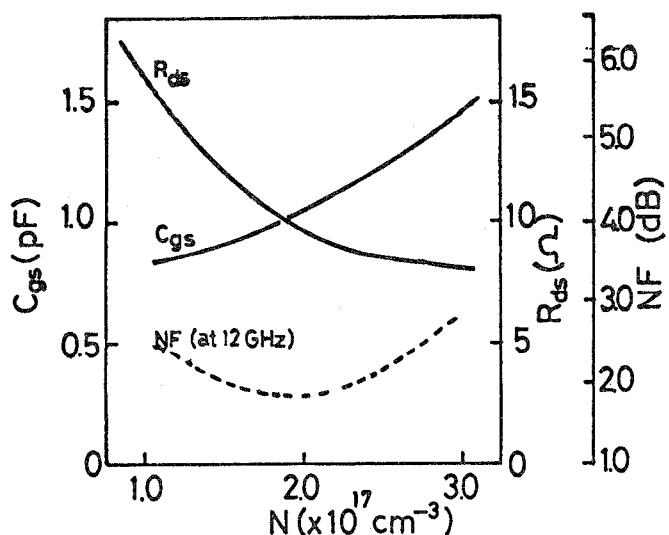


Fig. 3 C_{gs} at $V_g = 0$ V and $V_{ds} = 0$ V, and R_{ds} depending on the carrier density, N .

Optimized carrier density was 2×10^{17} cm^{-3} as shown in Fig. 3, where C_{gs} at the gate to source voltage (V_g) of 0 V and the drain to source voltage (V_{ds}) of 0 V and the source to drain resistance, R_{ds} , are shown as a function of the carrier density, N .

Fig. 4 shows pattern configuration of the FET chip fabricated basing on these design consideration. A deep gate recess structure was adopted for high reliability (3). Gate was aluminum of which length and thickness were 0.7 μm and 0.6 μm , respectively. Source and drain were metalized with Au-Ge/Ni and their spacing was 4 μm .

For packaged FETs, in order to prevent degradation of device performance at higher frequencies, methods of wire bonding were devised to minimize the lead inductance.

Electrical Characteristics

Fig. 5 shows the distribution of NF_{min} and G_a for packaged FETs fabricated from three lots of wafers. The statistic mean value and the standard deviation are 1.7 dB and 0.2 dB for NF_{min} and 11 dB and 0.5 dB for G_a , respectively at 12 GHz. As the best result, NF_{min} of 1.3 dB was obtained with G_a of 11 dB at the same frequency.

In Ku band, characteristics of NF_{min} of 2.1 dB and G_a of 9.3 dB at 15 GHz and NF_{min} of 2.4 dB and G_a of 7.5 dB at 18 GHz were reproducibly obtained as shown in Fig. 6.

A single stage amplifier was constructed using this packaged FET and a triplate strip line composed of teflon-fiberglass board of 0.8 μm thickness.

In the frequency range from 17.5 to 18.1

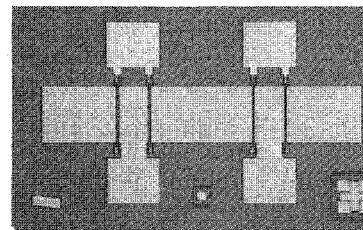


Fig. 4 Pattern configuration of the developed FETs chip.

GHz, this amplifier provided NF of 2.7 dB and G_a of 6.4 dB under the noise matching condition and G_a of 11 dB under the gain matching condition as shown in Fig. 7.

From the excellent performance in above X-band frequency range, these devices are believed to open a new stage in application for SHF TV broadcasting and satellite telecommunication.

Summary

Criteria in selecting GaAs epitaxial wafer and optimizing the device structure and configuration for super low noise GaAs FET operating above X band frequencies are described.

The packaged FETs fabricated basing on these considerations provided the statistic mean NF_{min} of 1.7 dB, the standard deviation of 0.2 dB at 12 GHz and NF_{min} of 2.4 dB at 18 GHz.

Using these FETs, a single stage amplifier with NF of 2.7 dB and G of 6.4 dB at 18 GHz was constructed.

Acknowledgement

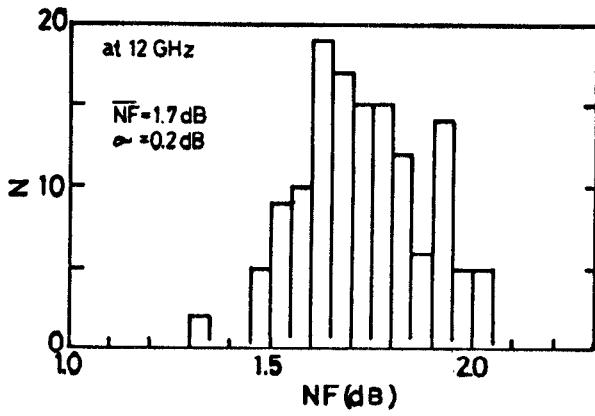
Authors wish to thank Drs. K. Shirahata and T. Ishii for useful suggestions and discussions.

Reference

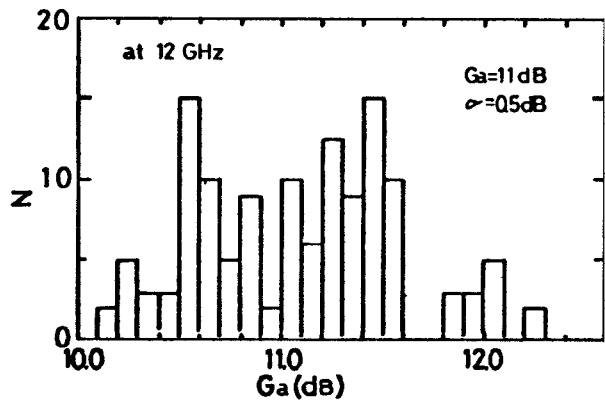
(1) C.L. Huang, S.L. Mason, R.W. Wong, L.J. Nevin and J.S. Barrera ; 1979 IEEE, ISSCC, p. 112.

(2) T. Suzuki, A. Nara, M. Nakatani, T. Ishii, S. Mitsui and K. Shirahata ; 1979 MTT-S IMS digest, p. 393.

(3) T. Suzuki, M. Otsubo, T. Ishii and K. Shirahata ; 1979 9th Eu.M.C., p. 331.



(a)



(b)

Fig. 5 Distribution of NF_{min} (a) and G_a (b) for packaged FETs fabricated from three lots of wafers .

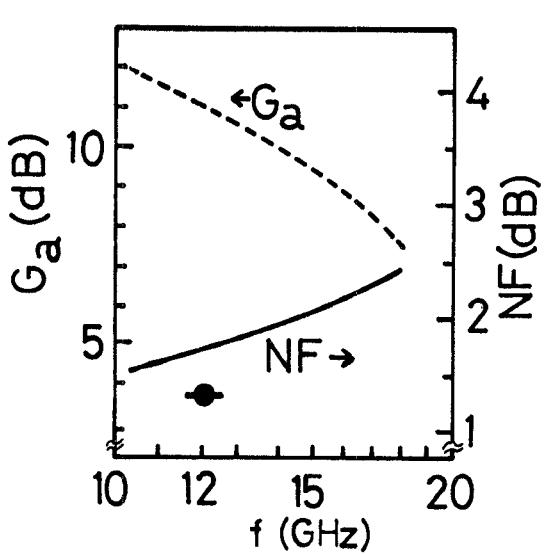


Fig. 6 NF_{min} and G_a depending on frequency.
● shows the state of the arts results.

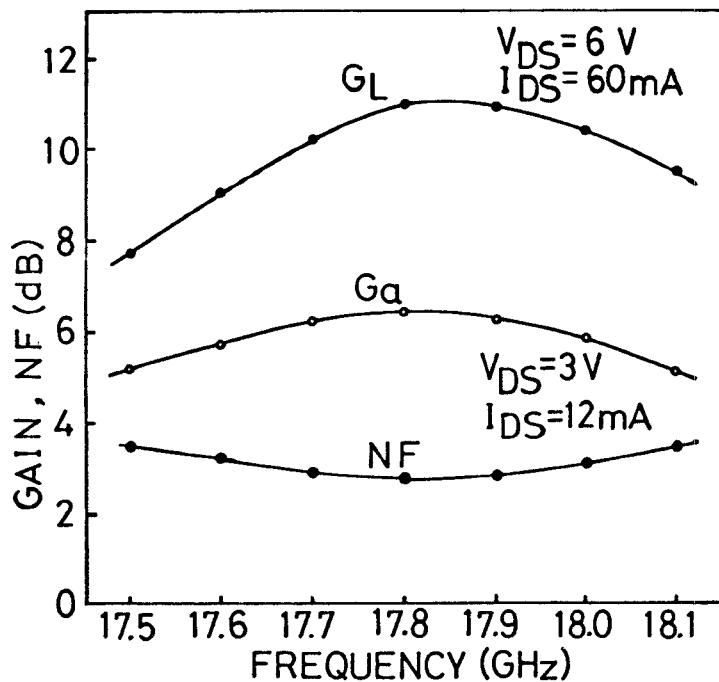


Fig. 7 RF characteristics of amplifier using the packaged FETs.